Modern power electronics products require small size and lighter weight of power electronics parts. Filter inductor and capacitor sizes must be small. With the small filter, the switching semiconductor devices must have small switching loss. And heat sink also must be reduced. For the safe operation with the small heat sink, the switching semiconductor devices must have small conduction loss. IXYS developed new generation of Trench MOSFET (Trench2™), which has small gate charge and low on-resistance. The MOSFET will be well suited for high power applications of synchronous DC to DC converters used in various systems. The MOSFET is rugged and has avalanche energy capability.

### Table 1: Few Examples of IXYS Trench2™ N-Channel Power MOSFETs

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Vdss (max) (V)</th>
<th>Id @ Tc=25°C (A)</th>
<th>Rds(on) @ Tj=25°C (Ω)</th>
<th>Ciss (pF)</th>
<th>Qg (nC)</th>
<th>trr @ Tj=25°C (ns)</th>
<th>R(th)JC (°C/W)</th>
<th>Pd (W)</th>
<th>EAS (mJ)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>IXTA220N04T2</td>
<td>40</td>
<td>220</td>
<td>0.0035</td>
<td>6500</td>
<td>112</td>
<td>45</td>
<td>0.42</td>
<td>360</td>
<td>600</td>
<td>TO-263</td>
</tr>
<tr>
<td>IXTP220N04T2</td>
<td>40</td>
<td>220</td>
<td>0.0035</td>
<td>6500</td>
<td>112</td>
<td>45</td>
<td>0.42</td>
<td>360</td>
<td>600</td>
<td>TO-220</td>
</tr>
<tr>
<td>IXTA90N055T2</td>
<td>55</td>
<td>90</td>
<td>0.0084</td>
<td>2670</td>
<td>42</td>
<td>37</td>
<td>1.0</td>
<td>150</td>
<td>300</td>
<td>TO-263</td>
</tr>
<tr>
<td>IXTP90N055T2</td>
<td>55</td>
<td>90</td>
<td>0.0084</td>
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<td>42</td>
<td>37</td>
<td>1.0</td>
<td>150</td>
<td>300</td>
<td>TO-220</td>
</tr>
<tr>
<td>IXTA110N055T2</td>
<td>55</td>
<td>110</td>
<td>0.0066</td>
<td>3060</td>
<td>57</td>
<td>38</td>
<td>0.82</td>
<td>180</td>
<td>400</td>
<td>TO-263</td>
</tr>
<tr>
<td>IXTP110N055T2</td>
<td>55</td>
<td>110</td>
<td>0.0066</td>
<td>3060</td>
<td>57</td>
<td>38</td>
<td>0.82</td>
<td>180</td>
<td>400</td>
<td>TO-220</td>
</tr>
<tr>
<td>IXTA200N055T2</td>
<td>55</td>
<td>200</td>
<td>0.0042</td>
<td>6800</td>
<td>109</td>
<td>49</td>
<td>0.42</td>
<td>360</td>
<td>600</td>
<td>TO-263</td>
</tr>
<tr>
<td>IXTP200N055T2</td>
<td>55</td>
<td>200</td>
<td>0.0042</td>
<td>6800</td>
<td>109</td>
<td>49</td>
<td>0.42</td>
<td>360</td>
<td>600</td>
<td>TO-220</td>
</tr>
<tr>
<td>IXTA70N075T2</td>
<td>75</td>
<td>70</td>
<td>0.012</td>
<td>2580</td>
<td>46</td>
<td>48</td>
<td>1.0</td>
<td>150</td>
<td>300</td>
<td>TO-263</td>
</tr>
<tr>
<td>IXTP70N075T2</td>
<td>75</td>
<td>70</td>
<td>0.012</td>
<td>2580</td>
<td>46</td>
<td>48</td>
<td>1.0</td>
<td>150</td>
<td>300</td>
<td>TO-220</td>
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<tr>
<td>IXTA90N075T2</td>
<td>75</td>
<td>90</td>
<td>0.010</td>
<td>3100</td>
<td>54</td>
<td>50</td>
<td>0.82</td>
<td>180</td>
<td>400</td>
<td>TO-263</td>
</tr>
<tr>
<td>IXTP90N075T2</td>
<td>75</td>
<td>90</td>
<td>0.010</td>
<td>3100</td>
<td>54</td>
<td>50</td>
<td>0.82</td>
<td>180</td>
<td>400</td>
<td>TO-220</td>
</tr>
</tbody>
</table>

**DC-to-DC Synchronous Converter Design:**

![Figure 1: Synchronous Buck Converter using IXYS Trench2™ Power MOSFET](image)
In Figure 1, the Q1 is called the high-side or control FET and Q2 is called the low-side or sync FET applied in a step-down DC to DC synchronous converter application. The ratio $V_o/V_{in}$ is controlled by the duty cycle of Q1. To improve the efficiency, it’s desirable to have Q2 turned ON when Q1 is turned OFF. A simplified switch state diagram is shown in Figure 2 [2]. It depicts the switching sequence as A-B-C-B-A where the state B called “dead time” when both Q1 and Q2 are OFF and the Schottky diode, D1 is ON to provide the freewheeling operation in the inductive load circuit. It’s desirable to reduce the dead time to a minimum to improve the efficiency. However, if the dead time is lower than the turn-on or turn-off times of Q1 and Q2, the circuit may go into state D, the shoot-through state when both Q1 and Q2 are ON at the same time causing a short-circuit in the input voltage source, Vin. The state D is undesirable since it would destroy transistors Q1 and Q2.

![Circuit Switch State Diagram](image-url)
The Switching Period, $T_S = T_{on} + T_{off}$, the Switching frequency, $f_S = \frac{1}{T_S}$

The duty cycle, $D = \frac{T_{on}}{T_S} = \frac{T_{on}}{T_{on} + T_{off}}$, Turn-on time, $T_{on} = DT_S$

Turn-off time, $T_{off} = (1 - D)T_S$.

An output DC voltage with lowest ripple is considered the best solution. Ripple appears in the output voltage as the L1 current’s ripple component, $\Delta I_{L1}(t)$, which charges and discharges the output capacitor, C1, as shown in Figure 4. C1 is charged during the
period when $I_{L1}(t)$ is greater than $I_o$. The charge ($\Delta Q$) that flows into $C1$ at this time divided by the value of $C1$ is the output voltage ripple component.

**Output Inductor Ripple Current and Voltage:**
The inductor voltage can be defined as,

$$V_L = L1 \frac{di}{dt} = Vin - Vo,$$

or, $\Delta I = \Delta I_{L1}(t) = \frac{\Delta t(Vin - Vo)}{L1}$, here, $\Delta t = Ton = DTs$

The inductor ripple current is,

$$\Delta I_{L1}(t) = DTs \frac{Vin - Vo}{L1} = \frac{D(Vin - Vo)}{f_s \cdot L1}$$  \hspace{1cm} (1)

The charge, $\Delta Q$, indicated in Figure 5, can be determined by calculating the area of the triangle with height $\frac{\Delta I_{L1}(t)}{2}$ and width $\frac{T_s}{2}$ shown in Figure 5.

$$\Delta Q = \frac{1}{2} \cdot \frac{\Delta I_{L1}(t)}{2} \cdot \frac{T_s}{2} = \frac{\Delta I_{L1}(t)}{8} \cdot \frac{T_s}{f_s}$$

The ripple voltage is,

$$\Delta V_L(t) = \frac{\Delta Q}{C1} = \frac{\Delta I_{L1}(t) T_s}{8C1} = \frac{D(1-D)Vin T_s^2}{8LIc1} = \frac{\pi^2 (1-D) Vo}{2} \cdot \frac{(f_c)^2}{f_s} = \Delta V_o(t)$$  \hspace{1cm} (2)

Where, $f_c = \frac{1}{2\pi \sqrt{LIc1}}$, Output low pass filter (LPF) resonant frequency, $f_s$ = The switching frequency. The inductor value of L1 and the effective series resistance (ESR) of the output capacitor, C1, affect the output ripple voltage, $\Delta V_L$. A capacitor with the lowest possible ESR is recommended for the application. For example, 4.7–10 uF capacitors in X5R/X7R technology have ESR approximately 10 mΩ.

**Summary of design equations:**
Ripples voltage/current, Inductor and Capacitor:

Output ripple voltage, $\Delta V_L(t) = \frac{\Delta I_{L1}(t) T_s}{8C1} = \frac{\Delta I_{L1}(t)}{8C1f_s}$  \hspace{1cm} (3)

Inductor ripple current, $\Delta I_{L1}(t) = 8C1f_s \cdot \Delta V_L(t)$  \hspace{1cm} (4)

Output inductor, $L1 \geq DTs \frac{Vin - Vo}{\Delta I_{L1}(t)} = \frac{D(Vin - Vo)}{f_s \cdot \Delta I_{L1}(t)}$  \hspace{1cm} (5)

Output capacitor, $C1 \geq \frac{\Delta I_{L1}(t)}{8f_s \Delta Vo}$ since $\Delta Q = \frac{1}{2} \cdot \frac{\Delta I_{L1}(t)}{2} \cdot \frac{T_s}{2} = C1 \cdot \Delta Vo$  \hspace{1cm} (6)

Output filter cut-off frequency, $f_c = \frac{1}{2\pi \sqrt{LIc1}}$  \hspace{1cm} (7)
Overview of Synchronous Converter Power Loss: [1]
The losses in the synchronous converter’s power switches can be defined by:

\[ P_{Total} = P_C + P_{SW} + P_{Gate} + P_{BD} \]  

(8)

Where \( P_C \) is the conduction loss, \( P_{SW} \) is the switching power loss, \( P_{Gate} \) is the gate drive loss and \( P_{BD} \) is the body diode loss. In addition, inductor equivalent DC resistance losses and output capacitor’s ESR loss play significant role in the converter design.

MOSFET Q1 and Q2’s Power Loss: [1]
The conduction losses: (replace D to 1-D for Sync FET, Q2):

\[ P_C = (I_D \sqrt{D})^2 \cdot R_{DS(on)} \]  

(9)

The gate-charge losses:

\[ P_{g-C} = V_G \cdot Q_g \cdot f_s \]  

(10)

The switching losses:

\[ P_{Switching} = P_{t(on)} + P_{t(off)} \]

\[ = \frac{[V_{DS(max)} \cdot t_{(on)} + I_{DS(0ff)} \cdot t_{(off)}]}{2} \cdot f_s \]  

(11)

MOSFET Body Diode Loss: [1]
The body diode loss is a function of dead time and in every switching cycle; there are two dead-time intervals, \( t_{d1} \) and \( t_{d2} \). The dead-time is defined as the time required when both the MOSFETs Q1 and Q2 are OFF in order to prevent shoot-through.
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We can write as:

\[ P_{BD} = P_{td1} + P_{td2} \]  \hspace{1cm} (12)

Where \( P_{td1} \) is the body diode loss during dead time \( t_{d1} \) and \( P_{td2} \) is the body diode loss during dead time \( t_{d2} \).

\[ P_{td1} = P_{cd1} + P_{rr1} = V_f \cdot \left( I_o - \frac{\Delta I_L}{2} \right) \cdot t_{d1} \cdot f_S + \frac{1}{2} \cdot V_{in} \cdot I_{rr} \cdot t_{rr} \cdot f_S \]  \hspace{1cm} (13)

\[ P_{td2} = P_{cd2} (P_{rr2} = 0) = V_f \cdot \left( I_o + \frac{\Delta I_L}{2} \right) \cdot t_{d2} \cdot f_S \]  \hspace{1cm} (14)

**PWM Gate Driver Power loss: [1]**

The power dissipation in the driver is defined by,

\[ P_{DRIVER} = Q_{(on)} \cdot V_{DD} \cdot f_S \]  \hspace{1cm} (15)

where \( Q_{(on)} \) is the total gate charge of the MOSFET and \( V_{DD} \) is the driver power supply.

The gate “point of voltage” is,

\[ V_{Sp} = V_{TH} + \frac{I_o}{g_{fs}} \]  \hspace{1cm} (16)

The driver current is,

\[ I_{DRIVER(L-H)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-UP)} + R_{Gate}} \]  \hspace{1cm} (17)

\[ I_{DRIVER(H-L)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-DOWN)} + R_{Gate}} \]  \hspace{1cm} (18)

The rise time is,

\[ t_{(on)} = \frac{Q_{(on)}}{I_{DRIVER(L-H)}} \]  \hspace{1cm} (19)

The fall time is,

\[ t_{(off)} = \frac{Q_{(on)}}{I_{DRIVER(H-L)}} \]  \hspace{1cm} (20)

If an external Schottky diode (D1) is used across Q2, the Schottky’s capacitance needs to be charged during Q1 turn-on. The power loss to charge the Schottky’s capacitance is,

\[ P_{C(SCHOTTKY)} = C_{SCHOTTKY} \cdot \frac{V_{IN}^2}{2} \cdot f_S \]  \hspace{1cm} (21)
Design Example 1:
Assume design parameters as \(V_{IN}=12\,\text{V}, \, V_O=3.3\,\text{V} \) and \(I_O=12\,\text{A}\).

Table 1: Design Consideration 1 for synchronous buck converter

<table>
<thead>
<tr>
<th>Input Voltage, Vin</th>
<th>12V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage, Vo</td>
<td>3.3V</td>
</tr>
<tr>
<td>Output Current, Io</td>
<td>12A</td>
</tr>
</tbody>
</table>

Assume the output ripple voltage is within \(\pm 1\% \) of \(V_O\). For \(V_O =3.3\,\text{V}\), the output ripple is limited within, \(\Delta V_L(t) \leq 0.033V\). When the output capacitor (\(C_1\)) is 10uF, the inductor \(L_1\) values for the range of switching frequencies from 100 kHz to 500 kHz are given in Table: 2 based on equations 3-7.

<table>
<thead>
<tr>
<th>(V_{IN}) (V)</th>
<th>(V_O) (V)</th>
<th>(D)</th>
<th>(\Delta V_L) (V)</th>
<th>(f_s) (kHz)</th>
<th>(C_1) (uF)</th>
<th>(\Delta I_{L1}) (A)</th>
<th>(L_1) (uH)</th>
<th>(f_c) (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>3.3</td>
<td>0.275</td>
<td>0.033</td>
<td>100</td>
<td>10</td>
<td>0.264</td>
<td>90</td>
<td>5.31</td>
</tr>
<tr>
<td>12</td>
<td>3.3</td>
<td>0.275</td>
<td>0.033</td>
<td>200</td>
<td>10</td>
<td>0.528</td>
<td>45.31</td>
<td>7.48</td>
</tr>
<tr>
<td>12</td>
<td>3.3</td>
<td>0.275</td>
<td>0.033</td>
<td>300</td>
<td>10</td>
<td>0.792</td>
<td>30.20</td>
<td>9.16</td>
</tr>
<tr>
<td>12</td>
<td>3.3</td>
<td>0.275</td>
<td>0.033</td>
<td>400</td>
<td>10</td>
<td>1.056</td>
<td>22.65</td>
<td>10.60</td>
</tr>
<tr>
<td>12</td>
<td>3.3</td>
<td>0.275</td>
<td>0.033</td>
<td>500</td>
<td>10</td>
<td>1.32</td>
<td>18.12</td>
<td>11.83</td>
</tr>
</tbody>
</table>

Synchronous Driver Controller: ISL6594D from Intersil:

Based on equation 18 and 19, From ISL6594D driver datasheet, given high-side: \(t_r=26\,\text{nS}\), \(t_f=18\,\text{nS}\) and source/sink current = 1.25/2A (max). For low-side, \(t_r=18\,\text{nS}\), \(t_f=12\,\text{nS}\) and source/sink current = 2/3.0 A (max):

Table 4: from Datasheet

<table>
<thead>
<tr>
<th>High-Side</th>
<th>Rise time</th>
<th>Source Current (A)</th>
<th>Required Qg(on)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>26 ns</td>
<td>1.25</td>
<td>32.5nC</td>
</tr>
<tr>
<td>Sink</td>
<td>18 ns</td>
<td>2</td>
<td>36nC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Low-Side</th>
<th>Rise time</th>
<th>Source Current (A)</th>
<th>Required Qg(on)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>18ns</td>
<td>2</td>
<td>36nC</td>
</tr>
<tr>
<td>Sink</td>
<td>12ns</td>
<td>3</td>
<td>36nC</td>
</tr>
</tbody>
</table>
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ISL6594D Specification:

Recommended devices for this application:

1. **IXTA90N055T2**
   
   VDS = 55V, Id25=90A
   
   Qg(on) = 42nC, Qgs = 14nC, Qgd = 8.5nC,
   
   td(on) = 19nS, tr = 21nS, td(off) = 39nS, tf = 19nS.
   
   Rds(on) = 8.4mΩ
   
   Vgs(th) = 2-4V, gfs = 43
   
   Ciss = 2670pF, Coss = 420pF, Crss = 100pF
   
   Or,
   
   1. **IXTA110N055T2**
      
   Vds = 55V, Id25=110A
   
   Qg(on) = 57nC, Qgs = 16nC, Qgd = 11nC,
   
   td(on) = 18nS, tr = 25nS, td(off) = 40nS, tf = 23nS.
   
   Rds(on) = 6.6mΩ, Vgs(th) = 2-4V, gfs = 49
   
   Ciss = 3060pF, Coss = 497pF, Crss = 105pF

Analysis based on Above IXTA90N055T2:

\[ Q_{G(SW)} = 8.5nC + \frac{14nC}{2} = 15.5nC \]

The “point of voltage” is defined by,

\[ V_{SP} = V_{TH} + \frac{I_d}{g_{fs}} = 3 + \frac{15}{43} = 3.35V \]

The driver current is,

\[ I_{DRIVER(L-H)} = \frac{V_{DD} - V_{SP}}{R_{DRIVER(PULL-UP)} + R_{Gate}} = \frac{10 - 3.35}{3 + 2} = \frac{6.65}{5} = 1.33A \]
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\[ I_{\text{DRIVER(H-L)}} = \frac{V_{DD} - V_{SP}}{R_{\text{DRIVER(PULL-DOWN)}} + R_{\text{Gate}}} = \frac{10 - 3.35}{2.2 + 2} = 1.58A \]

The rise time is, \[ t_{(\text{on})} = 26nS + 10nS = 36nS \]

The fall time is, \[ t_{(\text{off})} = 18ns + 10nS = 28nS \]

**High-Side MOSFET loss (Q1=IXTA90N055T2):**

The conduction loss is,
\[ P_{\text{Cond}_{-}Q1} = I_{O}^{2} \cdot R_{DS(on)} \cdot D \]
\[ = 12^{2} \cdot 0.0084 \cdot 0.275 = 0.332 = 332mW \]

The Gate-Charge losses: (assume \( f_s = 200 \) kHz)
\[ P_{G\text{C}_{-}Q1} = V_{GS} \cdot Q_g \cdot f_s = 10.0 \cdot 42 \cdot 10^{-9} \cdot 200 \cdot 10^{3} = 84mW \]

And estimated switching loss is,
\[ P_{t} = \frac{[V_{DS(max)} \cdot I_{DS(on)} \cdot t_{(on)} + I_{DS(off)} \cdot t_{(off)}] \cdot f_s}{2} \]
\[ = \frac{12 \cdot 12 (36 + 28) \cdot 10^{-9} \cdot 200 \cdot 10^{3}}{2} = 0.921W = 921mW \]

Total high-side losses: 332mW+84mW+921mW = 1337mW=1.337W

**Low-Side MOSFET loss (Q2):**

The conduction loss is,
\[ P_{\text{Cond}_{-}Q2} = I_{D}^{2} \cdot R_{DS(on)} \cdot (1 - D) \]
\[ = 12^{2} \cdot 0.0084 \cdot 0.725 = 0.877W = 877mW \]

The Gate-Charge loss:
\[ P_{G\text{C}_{-}Q1} = V_{GS} \cdot Q_g \cdot f_s = 10.0 \cdot 42 \cdot 10^{-9} \cdot 200 \cdot 10^{3} = 84mW \]

Total low-side losses: 877mW+84mW =961mW

**ISL6594D Driver loss:**

From datasheet: \( V_{DD} = 5V \)

Table 6: IXS839 Driver Output Stage from datasheet

<table>
<thead>
<tr>
<th>Driver pull up resistance</th>
<th>( R_{\text{DRIVER(PULL UP)}} )</th>
<th>3.0Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver pull down resistance</td>
<td>( R_{\text{DRIVER(PULL DOWN)}} )</td>
<td>2.2Ω</td>
</tr>
<tr>
<td>Driver gate resistance</td>
<td>( R_{\text{GATE}} )</td>
<td>2Ω</td>
</tr>
</tbody>
</table>
The power dissipation in the driver is defined by,

\[ P_{\text{DRIVER}} = \frac{T_J - T_a}{R_{thJC}} = Q_{G(\text{total})} \cdot V_{\text{DD}} \cdot f_{SW} \]

where \( V_{\text{DD}} = 10\text{V} \) and \( f_s = 200\text{ kHz} \) (assume for this case)

The estimated driver power dissipation, \( P_D \approx 42 \cdot 10^{-9} \cdot 10 \cdot 200 \cdot 10^3 = 84\text{mW} \)

**Dead-Time Power Loss:** [3]

The dead-time is defined as the time required when both the MOSFETs are off in order to prevent shoot-through. In this period, the Schottky diode (or integral body diode is forward-biased and provided a power loss defined by,

\[ P_{\text{BD}} = P_{\text{td1}} + P_{\text{td2}} = 297\text{mW} + 208\text{mW} = 505\text{mW} \]

**Synchronous Converter Efficiency:**

If we neglect inductor’s DC power loss and capacitor’s ESR loss then the total estimated power loss, \( P_{\text{loss}} = 1337\text{mW} + 1007\text{mW} + 84\text{mW} + 505\text{mW} = 2933\text{mW} = 2.933\text{W} \)

Given output power, \( P_o = V_o I_o = 3.3 \cdot 12 = 39.6\text{W} \)

Estimated input power, \( P_{\text{in}} = 39.6 + 2.933 = 42.6\text{W} \)

The efficiency is defined as,

\[ \eta = \frac{V_o I_o}{V_{\text{in}} \cdot I_{\text{in}}} = \frac{P_o}{P_{\text{in}}} \]
The estimated efficiency, $\eta = \frac{39.6}{42.6} = 0.93 = 93\%$.

**Estimated input current:**

If we assume only 93% efficiency, then the estimated input current can be obtained,

Estimated input current, $I_{in} = \frac{V_{o10}}{V_{in} \cdot \eta} = \frac{3.3 \cdot 12}{12 \cdot 0.93} = 3.5A$

**Bootstrap Circuit Design:** [3]

Selecting bootstrap circuit components are done with consideration of the electrical rating and characteristics of the high-side MOSFET (Q1).

The capacitance is defined by datasheet of IXS839 driver,

$$ C_{BST} = \frac{Q_{G(total)}}{\Delta V_{BST}} \quad (24) $$

Where $Q_{G(total)}$ is the total gate charge of high-side MOSFET (Q1), and $\Delta V_{BST}$ is the allowable voltage droop in Q1. Assume this voltage droop equal to 0.1V.

$$ C_{BST} = \frac{42nC}{200mV} = 0.210\mu F $$

The bootstrap diode and capacitor voltage rating should be

$$ V_{Bootstrap\_Diode\_Capacitor} > V_{IN} + V_{DD} $$

The average forward current is defined by,

$$ I_{F(Avg)} = Q_{G(total)} \cdot f_{SW} \quad (25) $$

$$ = 42 \cdot 10^{-9} \cdot 250 \cdot 10^3 = 10.5mA $$

**Bibliography**

